REMARKS

In the February 11, 2004 Office Action, the Examiner noted that claims 1-17 were pending in the application; objected to claim 2 due to perceived informalities; objected to claim 16 under 37 C.F.R. § 1.75; and rejected claims 1-17 under 35 U.S.C. § 103(a). In rejecting the claims, U.S. Patents 5,142,630 to Ishikawa; 4,881,170 to Morisada; and 5,963,721 to Shiell et al. (References A-C, respectively, in the November 18, 2002 Office Action) and 5,442,756 to Grochowski et al. (Reference A in the February 11, 2004 Office Action) were cited. Claims 1-17 remain in the case. The Examiner's rejections are traversed below.

Newly Cited Prior Art: U.S. Patent 5,442,756 to Grochowski et al.

Grochowski et al. patent is directed to a branch prediction and resolution apparatus for a superscalar computer processor. In the branched prediction apparatus illustrated in Fig. 1, cache 24 stores instructions obtained in prefetch stage 12 from memory (not shown), as described at column 7, lines 27-29. Branched prediction control apparatus 44 is supplied with history information by branch target buffer 32 and controls multiplexer 30 to select an address (see column 7, line 67 to column 8, line 5). Write back stage (WJ) 20 "includes apparatus for finalizing the executed instructions, including posting the results of the execution stage to the registers" (column 7, lines 35-38) and provides "a WJ target address, a next sequential WJ instruction address, and history information" (column 8, lines 26-28) to branch verification apparatus 34. When "the branch verification apparatus ... detects the branch misprediction ... a prefetch is initiated to fetch the correct branch target instruction ... and the D1, D2, and Ex stages are flushed" (column 14, lines 36-40).

Objections to Claims 2 and 16

In paragraph 2 on page 2 of the Office Action, the Examiner objected to claim 2, because the Amendment filed by certificate of mail on September 9, 2003 and entered by the Request for Continued Examination (RCE) filed by certificate of mail on November 9, 2003 (received by the USPTO on November 10, 2003) deleted "a" using strikethrough, which was not seen by the Examiner or clerk entering the claim amendment. In this Amendment, the "a" has been deleted using double brackets. Therefore, withdrawal of the objection to claim 2 is respectfully requested.

In paragraph 3 on page 2 of the Office Action, the Examiner objected to claim 16 as a substantial duplicate of claim 11. However, claim 16 recites a combination of means-plus-function elements, while claim 11 recites a combination of circuits. Thus, a court would apply

the sixth paragraph of 35 U.S.C. § 112 to interpret claim 16, but not claim 11, resulting in different scope of these claims. Therefore, it is submitted that claims 11 and 16 are not substantial duplicates and the objection should be withdrawn. If the Examiner disagrees, the Examiner is respectfully requested to contact the undersigned by telephone prior to issuing another Office Action to arrange an Examiner Interview for the purpose of discussing what is necessary to remove this objection.

Rejections under 35 U.S.C. § 103(a)

In paragraphs 5-42 on pages 2-20 of the Office Action, claims 1-3, 5, 6, 8-10, 12-15 and 17 were rejected under 35 U.S.C. § 103 as unpatentable over Ishikawa in view of Grochowski et al. On pages 3-4 and the first two lines of page 5, it was asserted that claim 1 was obvious from the combination of Ishikawa and Grochowski et al., because it was sufficient "to execute an instruction in... steps or stages to overlap execution of instructions, which increases instruction processing speed" (Office Action, page 4, 20-22) to meet the limitations recited in claim 1. However, nothing was cited in either Ishikawa, or Grochowski et al. related to "instruction execution by way of an out-of-order system" (claim 1, line 3) as recited in the preamble of all of the independent claims. It is assumed that this limitation was ignored because it was in the preamble. Therefore, all of the independent claims have been amended to include in the body of the claim a reference to the out-of-order system. All of the independent claims, except claims 11 and 16, have been amended to add the limitation "when the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system" (e.g., claim 1, lines 7-8).

There is no suggestion in Grochowski et al. that the parallel pipeline system disclosed therein has the ability to execute an instruction out of order. On the contrary, as noted above, Grochowski et al. flushes all of the parallel pipelines if a branch is mispredicted. Thus, Grochowski et al. does not teach or suggest the limitations recited in lines 4-17 of claim 1. Since the Examiner added Grochowski et al. to Ishikawa which was previously used by itself to reject these claims, the Examiner has acknowledged that Ishikawa does not teach or suggest these limitations. Similar limitations are recited in claims 9, 13, 14 and 17; therefore, it is submitted that claims 1, 9, 13, 14 and 17 and claims 2, 3, 5, 6 and 8 which depend from claim 1, patentably distinguish over the combination of Ishikawa in view of Grochowski et al. for the above reasons.

In paragraphs 19-26 and 35-38 on pages 8-12 and 16-18, the Examiner asserted that Ishikawa and Grochowski et al. made the limitations recited in claims 10, 12 and 15 obvious. However, as discussed above, it is submitted that these references fail to teach or suggest the operations recited as being performed by the storage and control circuits in claim 10 and the

similar limitations recited in claims 12 and 15. For the above reasons, it is submitted that claims 10, 12 and 15 patentably distinguish over Ishikawa in view of Grochowski et al.

In paragraphs 43-45 on pages 20 and 21, the Examiner rejected claims 4 and 7 under 35 USC § 103(a) as unpatentable over Ishikawa in view of Grochowski et al. and further in view of Morisada. As discussed in the Amendment filed by certificate of mail on March 18, 2003 and received by the U.S. Patent and Trademark Office on March 24, 2003, Morisada is directed to an instruction prefetch control apparatus which uses mode information, such as "a master mode, a privilege mode and a cache bypass mode" to access a main memory using the correct mode. Nothing was cited or has been found in Morisada regarding an out-of-order system for executing instructions. Therefore, it is submitted that claims 4 and 7 patentably distinguish over the prior art for the reasons discussed above with respect to claim 1.

In paragraphs 46-49 on pages 21-23 of the Office Action, claims 11 and 16 were rejected under 35 USC § 103(a) as unpatentable over Ishikawa in view of Shiell et al. and further in view of Grochowski et al. The limitations that have been added to claims 11 and 16 in this Amendment are different from the limitation added to the other independent claims, in that claims 11 and 16 now recite that the "instruction fetch ports ... operate by way of the out-of-order system" (e.g., claim 11, lines 6-7) and recite details of how the ports are used "by way of the out-of-order system" (e.g., claim 11, lines 9 and 11-12).

As discussed in the March 18, 2003 Amendment, Shiell et al. is directed to a micro-processor system with the capability to synchronize bus transactions and includes an out-of-order mode for executing instructions. Specifically, column 1, lines 41-55 and Figs. 1 and 2 of Shiell et al. were cited. However, the cited text in Shiell et al. merely describes what was prior art in 1996 when Shiell et al. was filed, and defines "out-of-order execution" as execution of "instructions based on their 'readiness' to execute, rather than strictly on program order "(column 1, lines 53-55). This definition is repeated at the beginning of the Detailed Description of the Preferred Embodiment section at column 3, line 61 to column 4, line 2. However, these statements and the rest of Shiell et al. does not provide implementation details for any out-of-order execution system that is prior art to the present invention. The limitations recited in all of the independent claims, including claims 11 and 16, recite details of how the out-of-order system is implemented according to the present invention. It is submitted that undo experimentation on the part of a person on ordinary skill in the art would be required to develop what is disclosed in Shiell et al. into a system that meets the limitations recited in the independent claims. Therefore,

it is submitted that all of the claims, including claims 11 and 16 patentably distinguish over Ishikawa in view of Shiell et al. and Grochowski et al.

Summary

It is submitted that the references cited by the Examiner, taken individually or in combination, do not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-17are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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